

Docket: P910328

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Yi Chou Chen

/

/

/ Examiner: Fenty, Jesse A

U.S. Serial No: 10/802,312

/

/ Group Art: 2815

Filed: March 17, 2004

/

/

For: METHOD OF FORMING A

/

CHALCOGENIDE MEMORY CELL

/

HAVING A HORIZONTAL

/

ELECTRODE AND A MEMORY

/

CELL PRODUCED BY THE METHOD

/

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION UNDER 37 C.F.R. 1.131

I, Yi Chou Chen, declare as follows:

1. I am the inventor of the claims of the above-identified patent application.

2. Prior to December 13, 2002, I conceived the invention of forming a chalcogenide memory cell having a horizontal electrode, with a small cross-sectional area that makes electrical contact with a chalcogenide memory element, to thereby form the memory cell, as described and claimed in the referenced application.

3. A document illustrating my idea, prepared by me before December 13, 2002, is attached as Exhibit A. I prepared another document, prior to December 13, 2002, and had it transmitted to one of Macronix' s patent law firms, Stout, Uxa, Buyan & Mullins, LLP, with a request and authorization that a U.S. patent application be prepared and filed on the material described in the other document. A copy of this other document is attached hereto as Exhibit B.

4. A patent application was subsequently prepared and filed by the law firm in the U.S. Patent and Trademark Office.

The below undersigned declares that all statements made of his own knowledge are true and that all statements made on information and belief are believed to be true, being duly warned that willful false statements and the like are punishable by fine or imprisonment, or both, (18 U.S.C. 1001) and may jeopardize the validity of the application or any patent issuing therefrom.

2/27/06
Date

Yi-Chou, Chen
Yi Chou Chen

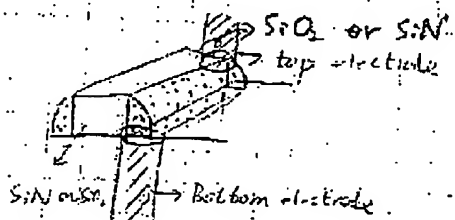
APPENDIX A

MACRONIX INTERNATIONAL 旺 宏 電 子

工作名稱: Super small cross-section chalcogenide cell
Ultra Structure

42

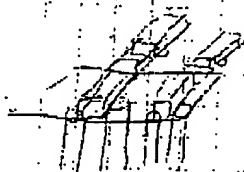
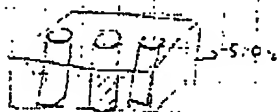
Structure:



Process:

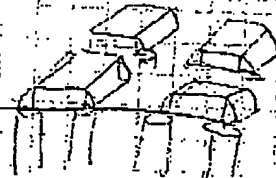
1. Bottom electrode

2. SiN/SiO₂ Dep / Photo / Etch



3. chalcogenide Dep / EB

3.5 / Etching
Photo to cut the
SiN and chalcogenide



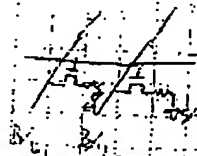
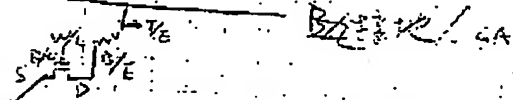
4. OXIDE / SiN Dep / Top electrode Photo / Etch



/ Top electrode Dep
(UV plating)

Transistor or P-N Diode

Circuit:



記錄人:

陳克成

日期:

[Redacted]

見證人:

何家驊
賴志

日期:

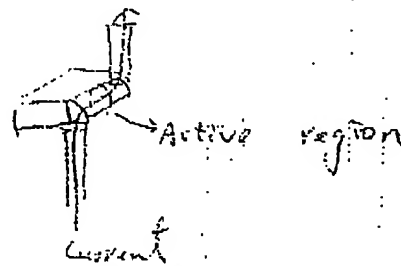
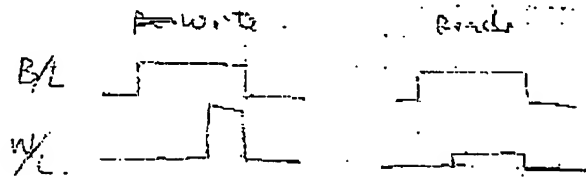
[Redacted]

MAC 旺 宏 電 子
MACRONIX INTERNATIONAL

工作名稱: (cont) 測試

43

Operation:



Pros. ① The cross-section of the chalcogenide is Ultra small.

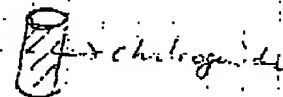
$$2. \text{ SiN thickness} = 1000 \text{ \AA}$$

$$\text{chalcogenide thickness} = 200 \text{ \AA}$$

$$\text{Then the Area} = 1000 \text{ \AA} \times 200 \text{ \AA} = 2 \times 10^5 \text{ \AA}^2$$

if chalcogenide is in a contact.

the diameter of the contact is



$$\frac{\pi}{4} D^2 = 2 \times 10^5$$

$$D = 504 \text{ \AA} \sim 0.05 \mu\text{m}$$

It's too difficult!!

for ~~248 nm~~ 133 nm

but using this tech. The limitation is no longer exist!
The diameter is determined by film thickness

3. 簽人: 陳逸舟

日期: [REDACTED]

見證人: 何永輝

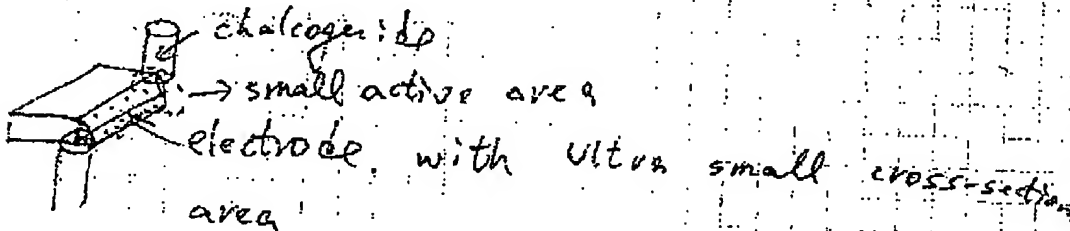
日期: [REDACTED]

賴新志

世 宏 電 子
MACRONIX INTERNATIONAL

工作名稱: Ultra small cross-section electrode
in chalcogenide memory

Replacing the chalcogenide by Metal / electrode
in the previous invention. And we can get
a Ultra small cross-sectional area in the
electrode



記錄人:

陳建舟

日期:

[REDACTED]

見證人:

賴昇志
何敬群

日期:

[REDACTED]

APPENDIX B

p910328

TITLE OF INVENTION

Definition of the contact area of electrode and phase change material in the chalcogenide phase-change memory

CLASSIFICATION: Method

**SUITABLE PRODUCT: Chalcogenide
Memory (Next generation memory)**

(This page will be provided by IPO)

BACKGROUND OF THE INVENTION

Field of the invention

The invention describes a innovative method to fabricate ultra small contact area between electrode and phase change material in the chalcogenide phase change memory. With this method, the contact area of the chalcogenide part and electrode will be ultra small, and as a result the current/power requirement of the chalcogenide memory dramatically decrease. The contact area of the chalcogenide part and electrode is defined by the thin film process and etching process in this invention.

The issues were solved and improvement by the invention

It is known that the chalcogenide phase change memory is not easy to be driven by CMOS circuit, because chalcogenide requires relatively high current to change its phase. Reducing the cross-sectional area of chalcogenide or electrode can reduce the current requirement directly. Many structures has been invented to reduce area. For example, to fabricate a ultra small contact hole and place the chalcogenide into the contact. However, these inventions basically are limited by lithography. Furthermore, it is very difficult to place materials into ultra small and deep holes. In this invention, contact area of the chalcogenide part and electrode is defined by the thin film process and etching process. Therefore, the lithography is no longer the limit. It is also not necessary to place materials into ultra small holes. Moreover, contact area of the chalcogenide part and electrode is ultra small. As a result, the current/power requirement of the chalcogenide memory is dramatically decreased.

SUMMARY OF THE INVENTION

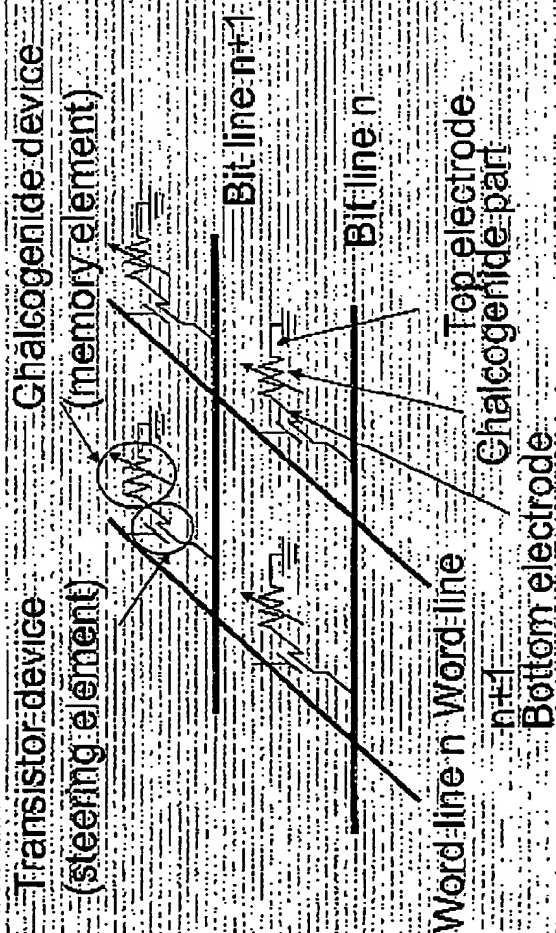
□ How this invention solves existing problems and achieves the objects

■ The contact area of the chalcogenide part and electrode is defined by 1. electrode film thickness and 2. The thickness of pad layer. With well control of film thickness, the area will be very small. Therefore the current required in the chalcogenide phase-change memory is reduced.

BRIEF DESCRIPTION OF DRAWING

RELATED DRAWINGS

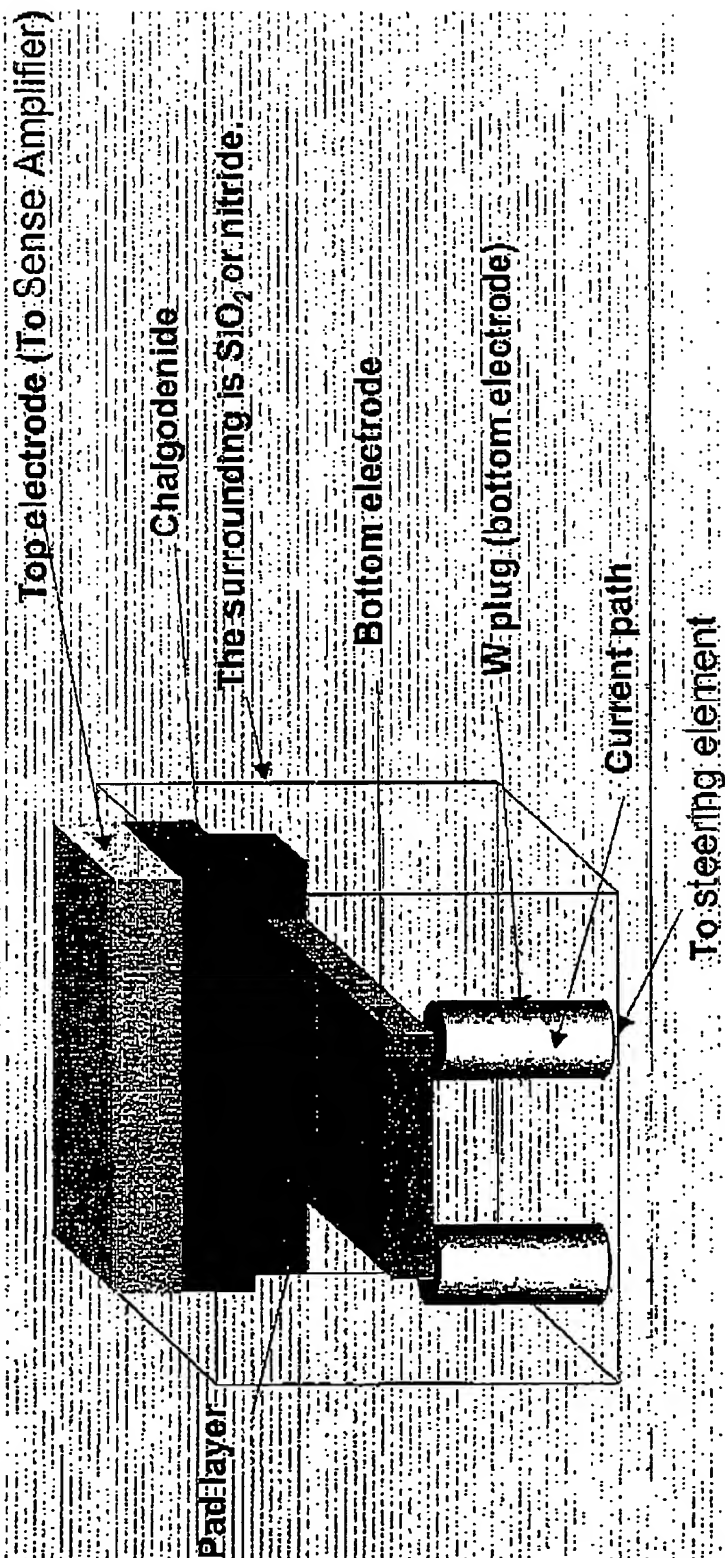
- A drawing of typical chalcogenide memory array.



BRIEF DESCRIPTION OF DRAWING

RELATED DRAWINGS

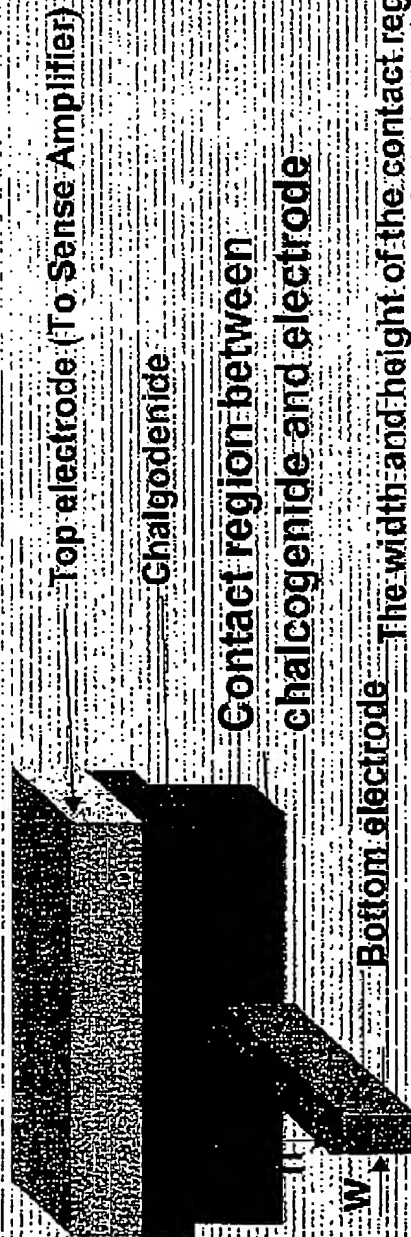
- A model of the invention.



BRIEF DESCRIPTION OF DRAWING

RELATED DRAWINGS

A model of the invention.



The width and height of the contact region between chalcogenide and electrode are defined by thin film and etching processes.

W: width of the bottom electrode.

H: height of the bottom electrode.

L: length of the bottom electrode.

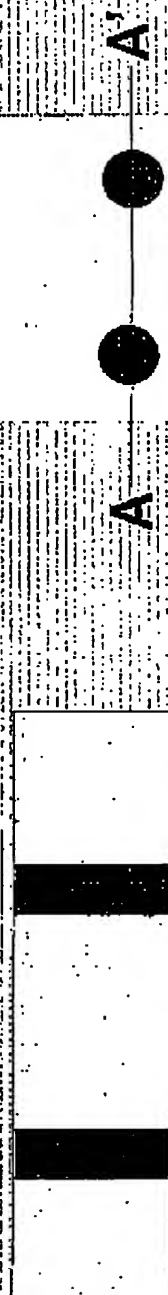
BRIEF DESCRIPTION OF DRAWING

RELATED DRAWINGS

■ Process flow

□ After regular CMOS process and W plug

AA' cross-section Plan view (4 cells)



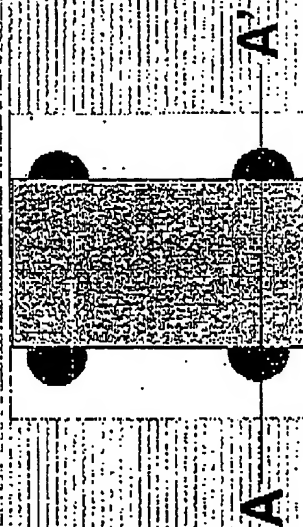
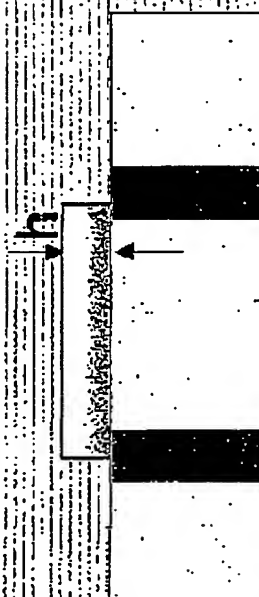
BRIEF DESCRIPTION OF DRAWING

□ RELATED DRAWINGS

- Pad layer (SLAB/ PHOTO/ ETCHING) Pad layer can be SiN, SiO₂, or SiON, etc.
- This process defines the height (h) of the bottom electrode.

AA' cross-section

Plan view (4 cells)



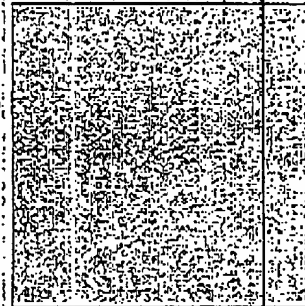
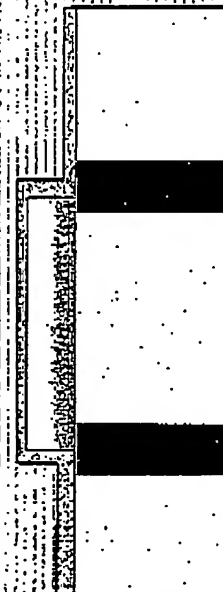
BRIEF DESCRIPTION OF DRAWING

RELATED DRAWINGS

- bottom electrode layer deposition (it can be TaN, TiN, TiW, Ti, W, poly or the combinations of above)

AA' cross-section

Plan view (4 cells)



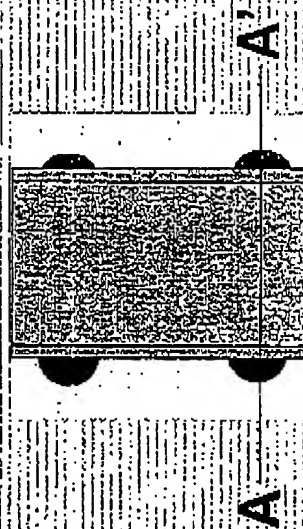
BRIEF DESCRIPTION OF DRAWING

RELATED DRAWINGS

- ☐ Etching Back of bottom electrode
- ☐ Current and last processes define the width (w) of the chalcogenide part.

AA' cross-section

Plan view (4 cells)



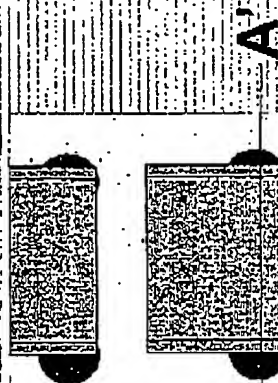
BRIEF DESCRIPTION OF DRAWING

RELATED DRAWINGS

□ Bottom electrode cutting(Photo/Etching)

AA' cross-section

Plan view (4 cells)



BRIEF DESCRIPTION OF DRAWING

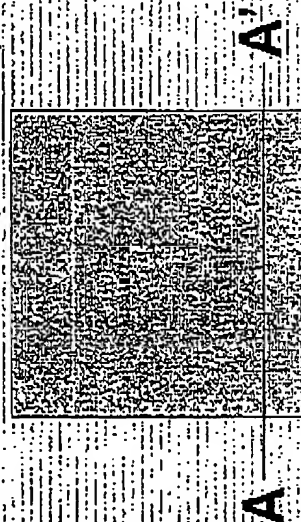
RELATED DRAWINGS

- Cap layer Deposition (it can be SiON, SiO₂, ZnS-SiO₂, etc.)

AA' cross-section



Plan view (4 cells)



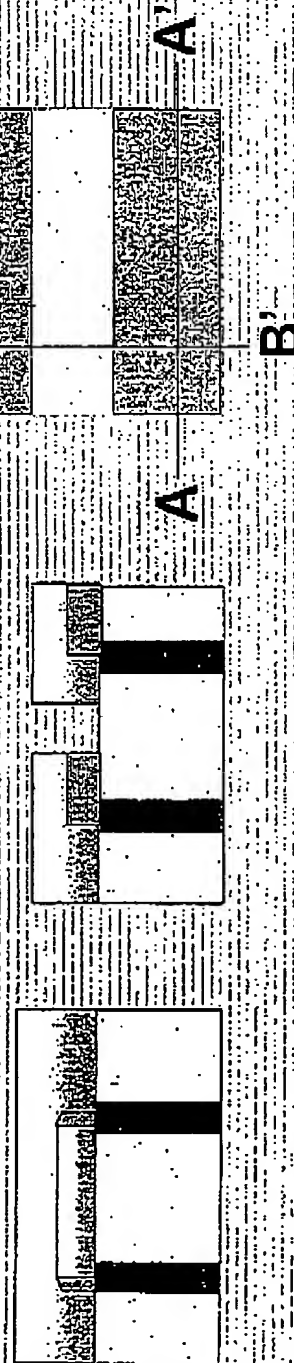
BRIEF DESCRIPTION OF DRAWING

RELATED DRAWINGS

- ☐ Routing: Photo/Etching
- ☐ Etching process should cut the electrode again.
- ☐ This process defines length (L) of the bottom electrode

Plan view (4 cells)

AA' cross-section BB' cross-section



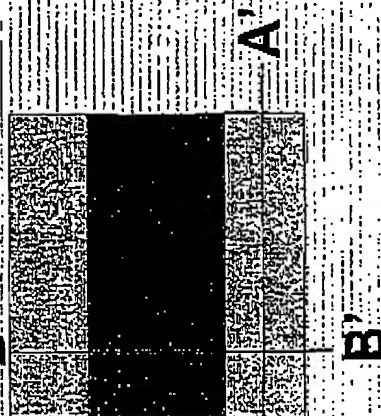
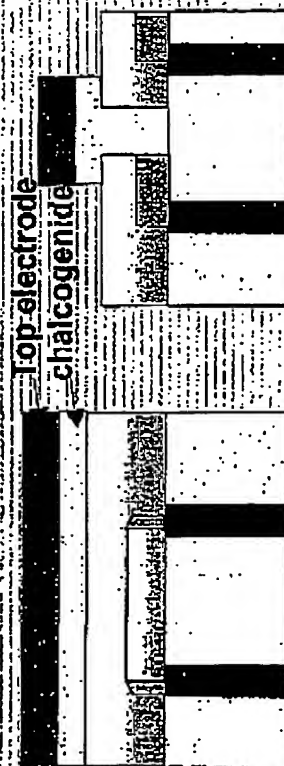
BRIEF DESCRIPTION OF DRAWING

RELATED DRAWINGS

- Routing 2: Chalcogenide and top electrode dep/Photo/Etching

Plan view (4 cells)

AA' cross-section BB' cross-section



PRIOR ART REFERENCE

	Classification	Patent No	Title	Remark
Prior art 1	Patent	US6111264	Small pores defined by a disposable internal spacer for use in chalcogenide memories	Similar to US6189582
Prior art 2	Patent	US6031287	Contact structure and memory element incorporating the same	
Prior art 3	Patent	US6114713	Integrated circuit memory cell having a small active area and method of forming same	

• CATEGORY: ESSAY, PAPER, PATENT, PRODUCT, ETC

COMPARING RELATED PRIOR ART WITH THIS INVENTION

Prior art	Disadvantages of the related Prior art	Differences from this invention
Prior art 1	<p>1- Dielectric layer can reduce the pore size, but the shrinking ratio is not unlimited. Because overhang may seal the hole. Therefore, the pore size can be limited by lithography. It is difficult to scale down.</p> <p>2- It's very difficult to control the size uniformity of ultra small pores with this method.</p> <p>3- It's very difficult to place chalcogenide into the holes.</p>	<p>1- The current is limited by chalcogenide.</p> <p>2- The minimal current path cross sectional areas defined by photothin film etching processes.</p>

COMPARING RELATED PRIOR ART WITH THIS INVENTION

	Disadvantages of the related Prior art	Difference from this invention
Prior art 2	<p>1. Electrode area can be reduced by this method, but the shrinking ratio is limited by the film thickness and photo. For example, if pore diameter is 0.15 μm and film thickness is 200A, the shrinkage ratio is only about 50%. It is difficult to scale down.</p> <p>2. Because the process needs to place electrode and oxide into small contacts, it is very difficult to process.</p>	<p>1. The bottom electrode is vertical and placed in a hole.</p> <p>2. The cross-sectional area of chalcogenide is defined by photo/thin film processes.</p>

COMPARING RELATED PRIOR ART WITH THIS INVENTION

	Disadvantages of the related Prior art	Difference from this invention
Prior art 3	1. It is very difficult to control the electrode area	1. The cross-sectional area of chalcogenide is defined by photoetching processes

THE SCOPE OF THE PROTECTION OF THE PATENT

□ Main Feature of the Invention

- The contact area between the chalcogenide and electrode is defined by 1. electrode film thickness and 2. The thickness of pad layer. With well control of film thickness, the area will be very small. Therefore the current required in the chalcogenide phase change memory is reduced.

□ The advantages of the invention

- Ultra-small contact area between the chalcogenide and electrode.
- Easy to fabricate. (Do not need to place materials into small pores)
- Easy to scale down. (The scaling limit of thin film and etching is less than 50A in 0.25um technology.)
- Take an easy calculation as an example:
If the PAD layer thickness is 500A and the electrode layer thickness is 200A, which is easy to fabricate by 0.25um process, the contact area is less than 10^{-5} A^2 . This is the cross section of a 0.036 um contact, which is almost impossible to fabricate nowadays.



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